AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "SUMMARY" in its entirety are substitute the following section therefor:

SUMMARY OF THE INVENTION

Accordingly, it is a feature of the present invention to provide an apparatus in a microprocessor for executing programmed native instructions that are provided directly to the microprocessor via an external instruction bus. The apparatus includes instruction translation logic and bypass logic. The instruction translation logic retrieves macro instructions provided via the external instruction bus, and decodes each of the macro instructions into associated native instructions for execution by the microprocessor, wherein the instruction translation logic decodes a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the programmed native instructions, and wherein the memory address is explicitly prescribed by contents of an architectural register, the contents and the architectural register being prescribed by a macro instruction. The bypass logic is coupled to the instruction translation logic. The bypass logic disables the instruction translation logic upon detection of the native bypass macro instruction, and provides the programmed native instructions for execution by the microprocessor, thereby bypassing the instruction translation logic.

In another aspect, it is a feature of the present invention to provide an apparatus that allows a micro instruction to be directly provided from an external instruction bus to execution logic within a pipeline microprocessor. The apparatus has a translator and bypass logic. The translator receives macro instructions from a macro instruction bus, and translates each of the macro instructions into associated micro instructions, where the associated micro instructions are provided to the execution logic via a micro instruction bus, and where the translator translates a native bypass macro instruction into an unconditional jump native instruction directing that program control be transferred to a memory address containing the micro instruction, and where the memory address is explicitly prescribed by contents of an architectural register. The contents the